art to which this disclosure belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the disclosure, and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0057] Exemplary embodiments are described herein with reference to cross section illustrations that are schematic illustrations of idealized embodiments. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments described herein should not be construed as limited to the particular shapes of regions as illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, a region illustrated or described as flat may, typically, have rough and/or nonlinear features. Moreover, sharp angles that are illustrated may be rounded. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region and are not intended to limit the scope of the claims.

[0058] Hereinafter, exemplary embodiments of the invention will be described in detail with reference to the accompanying drawings.

[0059] FIG. **1** is a top plan view of a display device according to an exemplary embodiment. As shown in FIG. **1**, an exemplary embodiment of a display device includes a display panel DP, a gate driving circuit **100**, a data driving circuit **200**, and a signal controller **300**.

[0060] The display panel DP is not limited to a particular type, and may be one of various display panels, for example, a liquid crystal display panel, an organic light emitting diode display panel, an electrophoretic display panel, an electrowetting display panel, and the like. Hereinafter, for convenience of description, an exemplary embodiment where the display panel DP is a liquid crystal display panel will be described in detail. In such an embodiment, the display device is a liquid crystal display including the liquid crystal display panel, and the display device may further include a polarizer (not illustrated), a backlight unit, and the like.

[0061] The display panel DP includes a first substrate DS**1**, a second substrate DS**2** that is disposed apart from the first substrate DS**1**, and a liquid crystal layer (referred to as LCL of FIG. **3**) that is disposed between the first substrate DS**1** and the second substrate DS**2**. In such an embodiment, the display panel DP includes a display area DA where a plurality of pixels PX**11** to PXnm are disposed, and a non-display area NDA that surrounds the display area DA, when viewed from the top plane view as shown in FIG. **1**.

[0062] The display panel DP includes a plurality of gate lines GL**1** to GLn and a plurality of data lines DL**1** to DLm that crosses the gate lines GL**1** to GLn. The plurality of gate lines GL**1** to GLn is connected to the gate driving circuit **100**. The plurality of data lines DL**1** to DLm is connected to the data driving circuit **200**. In FIG. **1**, for convenience of illustration, only some (GL**1** and GLn) of the plurality of gate lines GL**1** to GLn and only some (DL**1** and DLm) of the plurality of data lines DL**1** to DLm are illustrated.

[0063] Also, in FIG. **1**, for convenience of illustration, only some (PX**11**, PX**1***m*, PXn**1**, and PXnm) of the plurality of pixels PX**11** to PXnm are illustrated. Each of the plurality of pixels PX**11** to PXnm is connected to a corresponding gate line among the plurality of gate lines GL**1** to GLn and a corresponding data line among the plurality of data lines DL**1** to DLm.

[0064] The plurality of pixels PX**11** to PXnm may be divided into a plurality of groups depending on a display color thereof. Each of the plurality of pixels PX**11** to PXnm may display one of primary colors. The primary colors may include red, green and blue. However, exemplary embodiments are not limited thereto. Alternatively, the primary colors may further include various colors such as yellow, cyan, magenta, white, and the like.

[0065] The gate driving circuit **100** and the data driving circuit **200** receive controls signals from the signal controller **300**. The signal controller **300** may be disposed on or installed in a main circuit board MCB. The signal controller **300** receives image data and control signals from an external graphics controller (not shown). The control signals may include a vertical synchronization signal that determines frame sections, a horizontal synchronization signal that is a row distinction signal in one frame, a data enable signal that has a high level only for a section during which data is output, and clock signals.

[0066] The gate driving circuit **100** generates gate signals based on a control signal (hereinafter referred to as a gate control signal) received through a signal line GSL from the signal controller **300**, and outputs the gate signals to the plurality of gate lines GL**1** to GLn. In an exemplary embodiment, the gate driving circuit **100** may be provided or formed with the pixels PX**11** to PXnm through a same thin film process. In one exemplary embodiment, for example, the gate driving circuit **100** may be disposed in the non-display area NDA in the form of an amorphous silicon thin film transistor ("TFT") gate driver circuit ("ASG") or in the form of an oxide semiconductor TFT gate driver circuit ("OSG").

[0067] FIG. **1** shows an exemplary embodiment including a single gate driving circuit **100** connected to left ends of the plurality of gate lines GL**1** to GLn. In an alternative exemplary embodiment, the display device may include two gate driving circuits. In such an embodiment, one of the two gate driving circuits may be connected to the left ends of the plurality of gate lines GL**1** to GLn, and the other of the two gate driving circuits may be connected to the right ends of the plurality of gate lines GL**1** to GLn. In such an embodiment, one of the two gate driving circuits may be connected to odd-numbered gate lines, and the other of the two gate driving circuits may be connected to even-numbered gate lines.

[0068] The data driving circuit **200** generates gray voltages corresponding to the image data supplied from the signal controller **300** based on a control signal (hereinafter, will be referred to as a data control signal) received from the signal controller **300**. The data driving circuit **200** outputs the gray voltages to the plurality of data lines DL**1** to DLm as data voltages.

[0069] The data voltages may include positive data voltages having positive values with respect to a common voltage and/or negative data voltages having negative values with respect to the common voltage. Some of data voltages applied to the data lines DL**1** to DLm during the respective periods may be positive, and others of the data voltages applied to the data lines DL**1** to DLm during the respective periods may be negative. Polarity of the data voltages may be inverted on a frame-by-frame basis or a line-by-line basis